

FIG. 1A

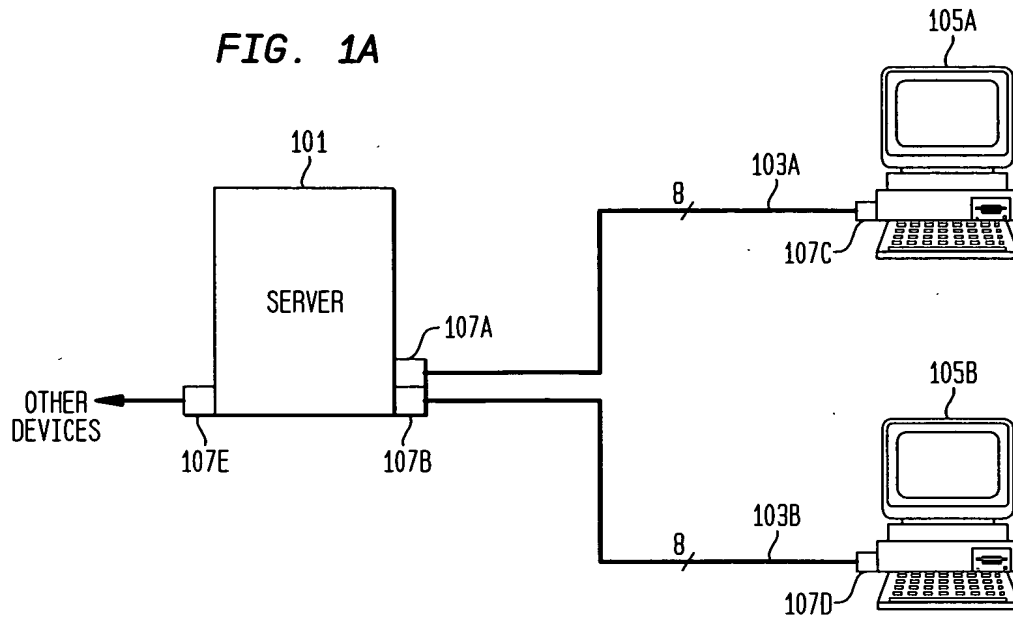
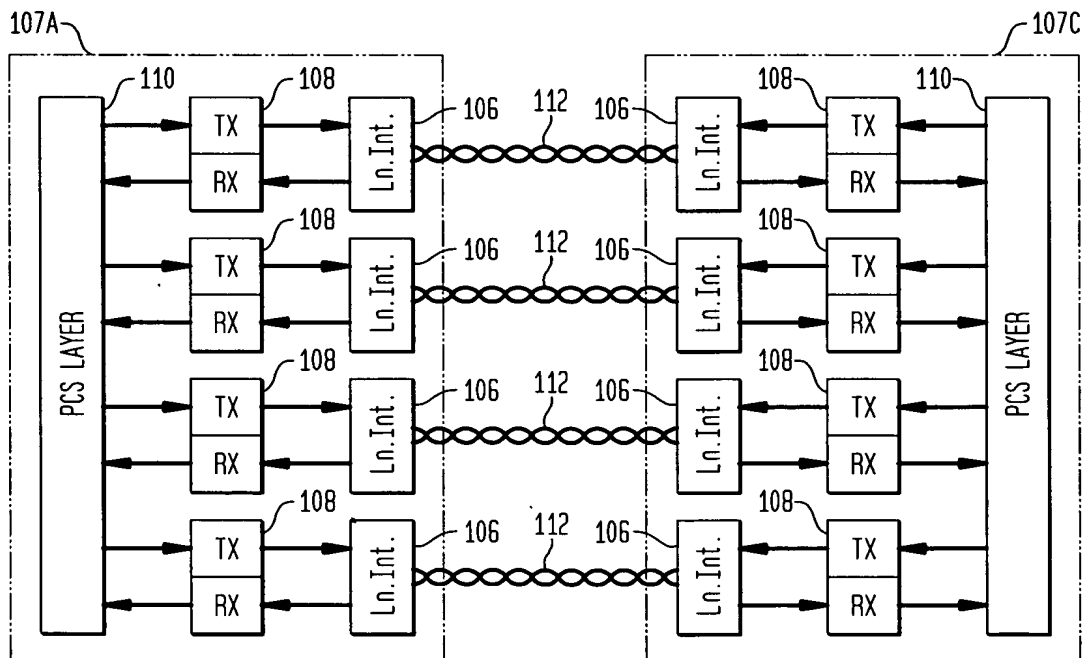
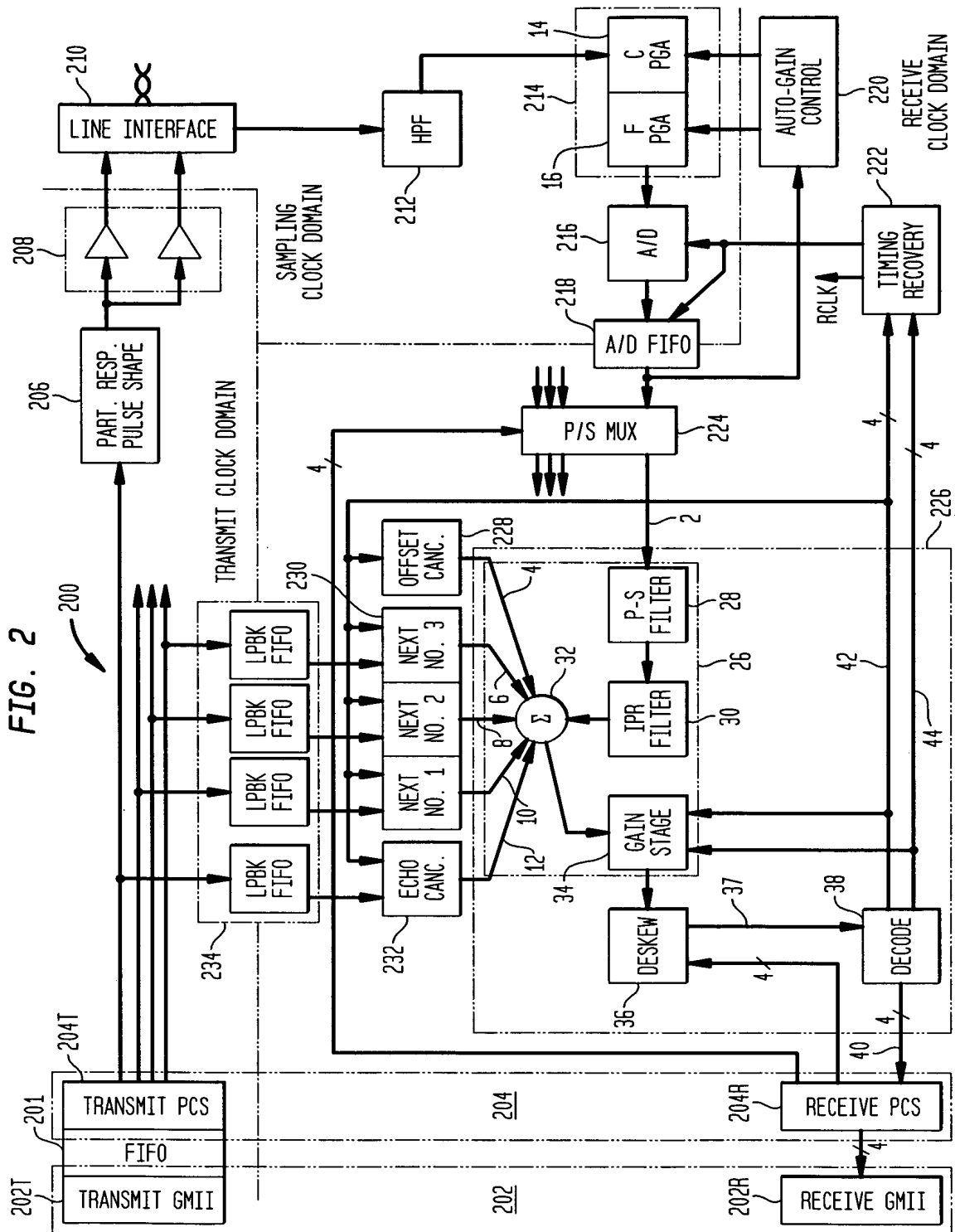


FIG. 1B





**FIG. 3**

```
graph LR
    210[LINE INTERFACE] --> 212[HIGH PASS FILTER]
    212 --> 214
    subgraph 214 [ ]
        16[COURSE PGA] --> 14[FINE PGA]
    end
    220[AUTOMATIC GAIN CONTROL] -- "4 BIT" --> 16
    220 -- "5 BIT" --> 14
    14 --> 216[A/D]
    216 --> 218[A/D FIFO]
    218 --> 220
    222[SET POINT] --> 220
```

**FIG. 4**

The circuit diagram shows a differential-mode input stage. It features two input buffers, 403 and 413, each with an input (IN) and an output (OUT). The output of buffer 403 is connected to the IN of switch 404 (SW1) and to resistor R405. The output of buffer 413 is connected to the IN of switch 411 (SW2) and to resistor R407. The control inputs (cntl) of switches 404 and 411 are connected to Vc1 and Vc2, respectively. The outputs (OUT) of switches 404 and 411 are connected to the IN of buffer 413 and to resistor R417. Resistor R417 is connected to a DC voltage source V1 (vdc = Vcm) and to ground (gnd). The circuit is labeled with various components: 401 (input), 403 (buffer), 404 (SW1), 405 (R405), 407 (R407), 411 (SW2), 413 (buffer), 415 (output), 417 (R417), 419 (V1), and gnd.

FIG. 5

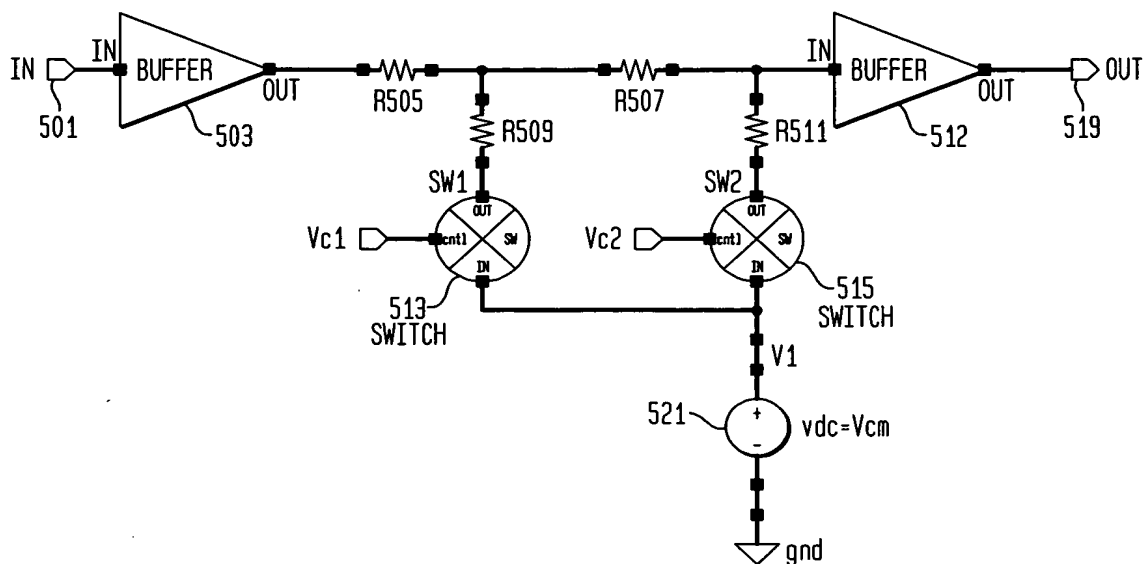


FIG. 6

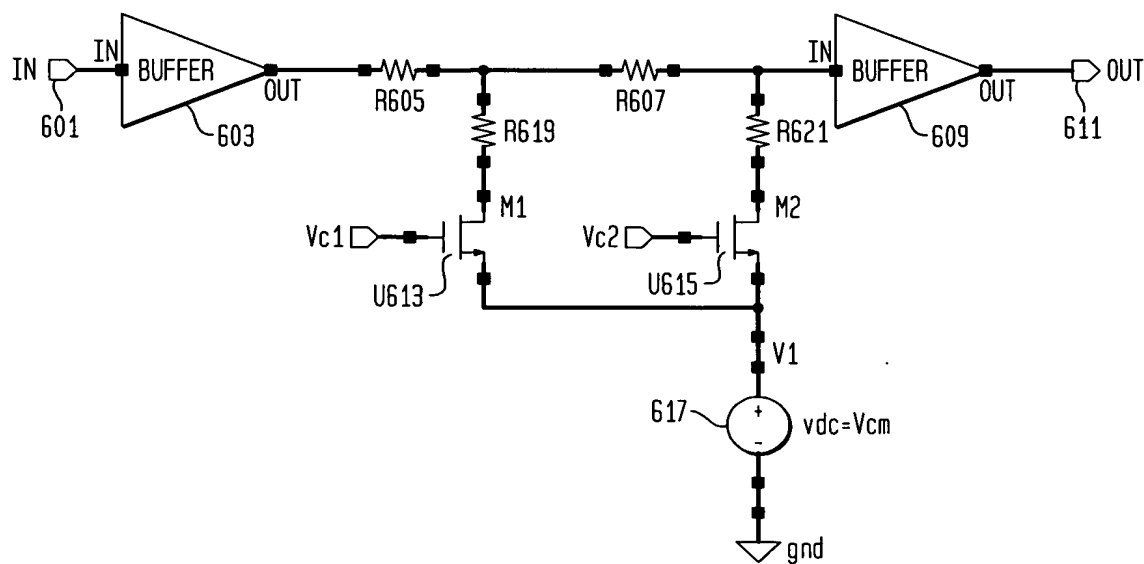
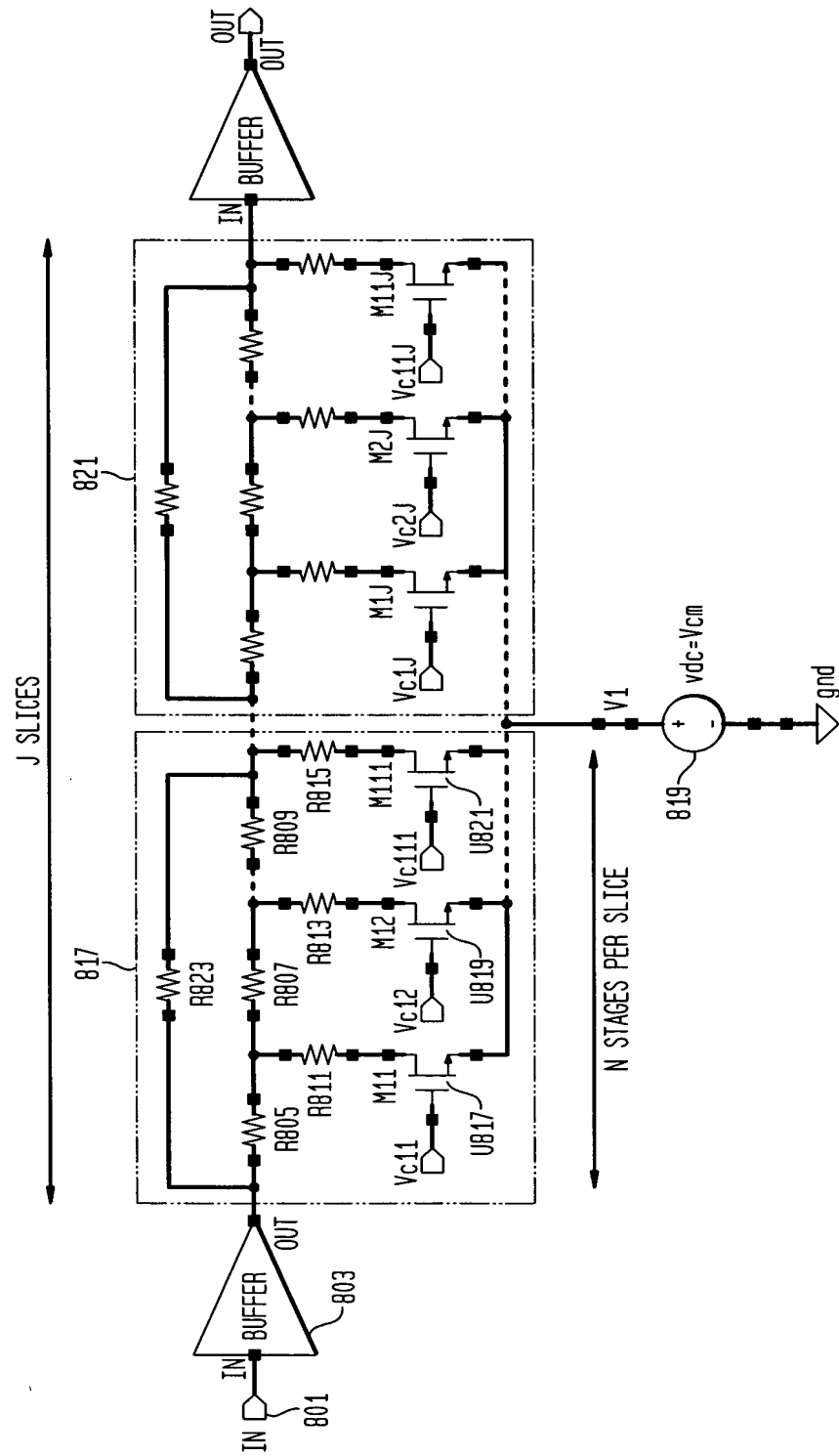
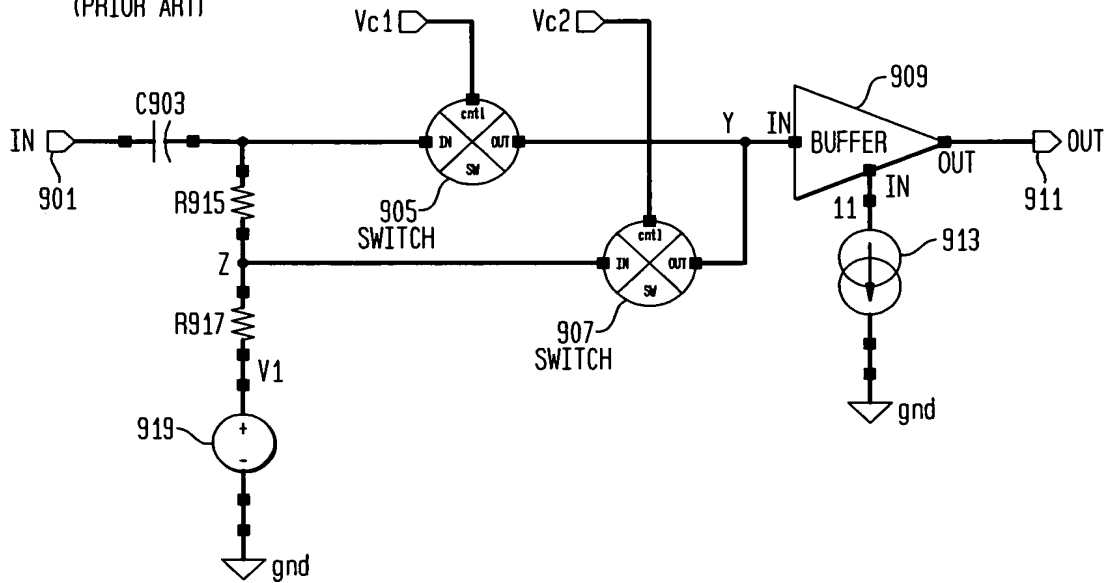




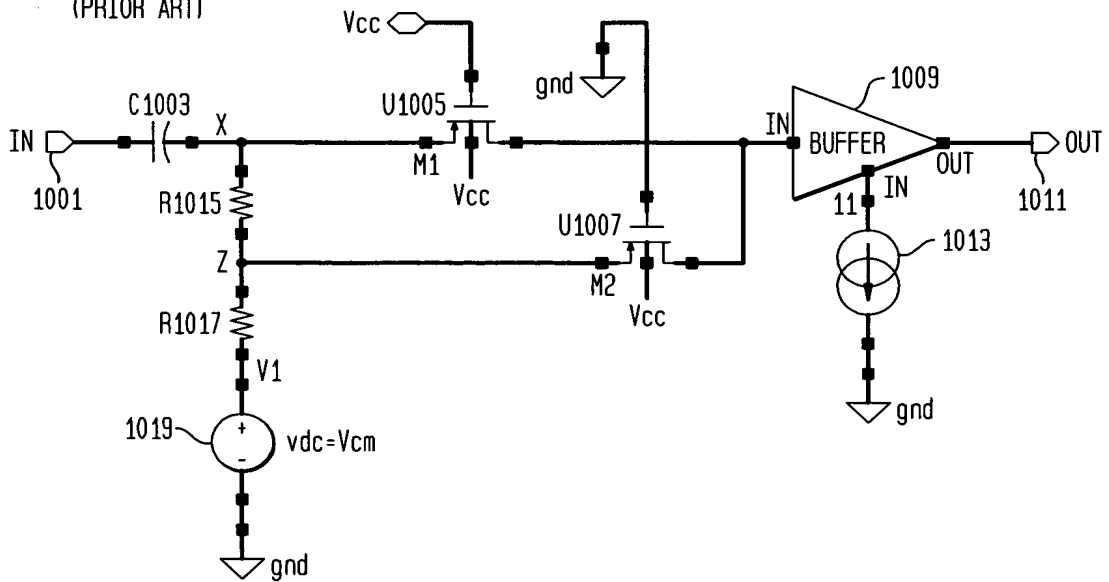
FIG. 8

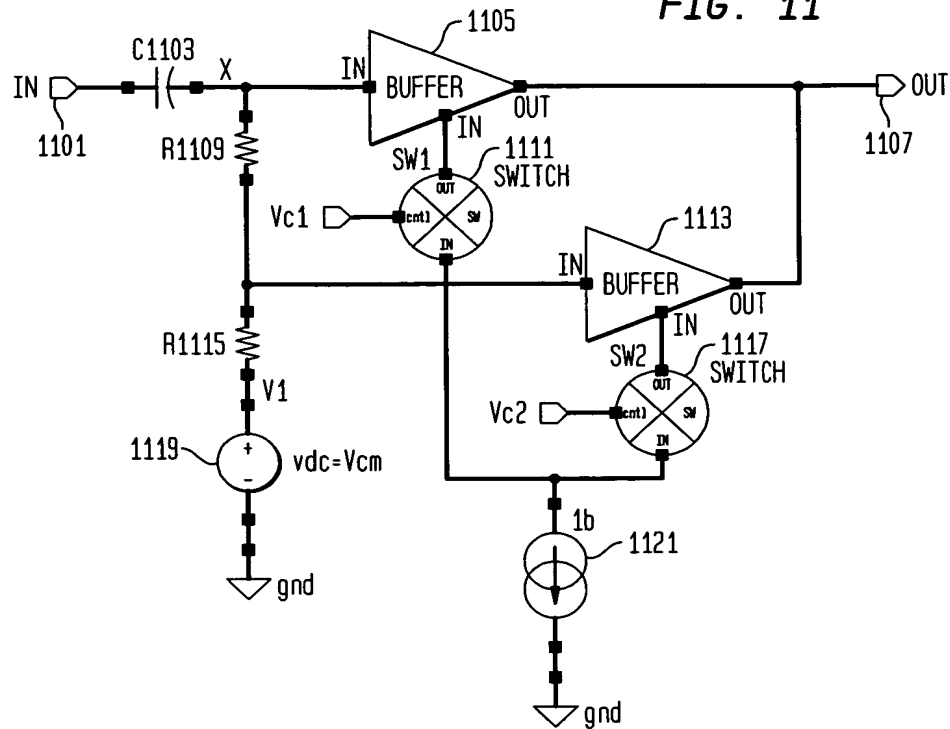
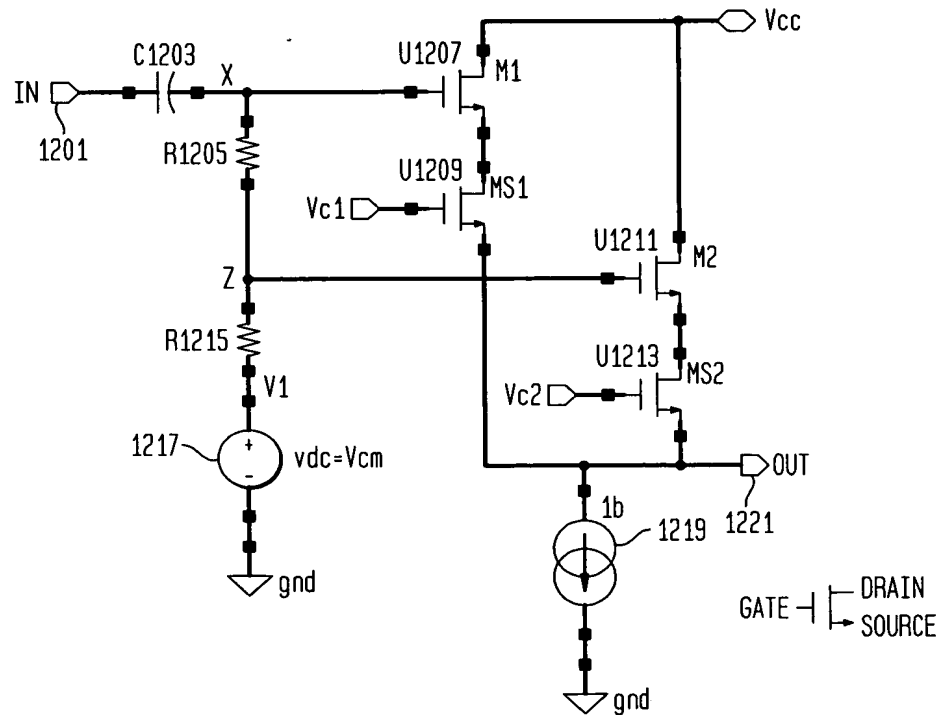


**FIG. 9**  
 (PRIOR ART)

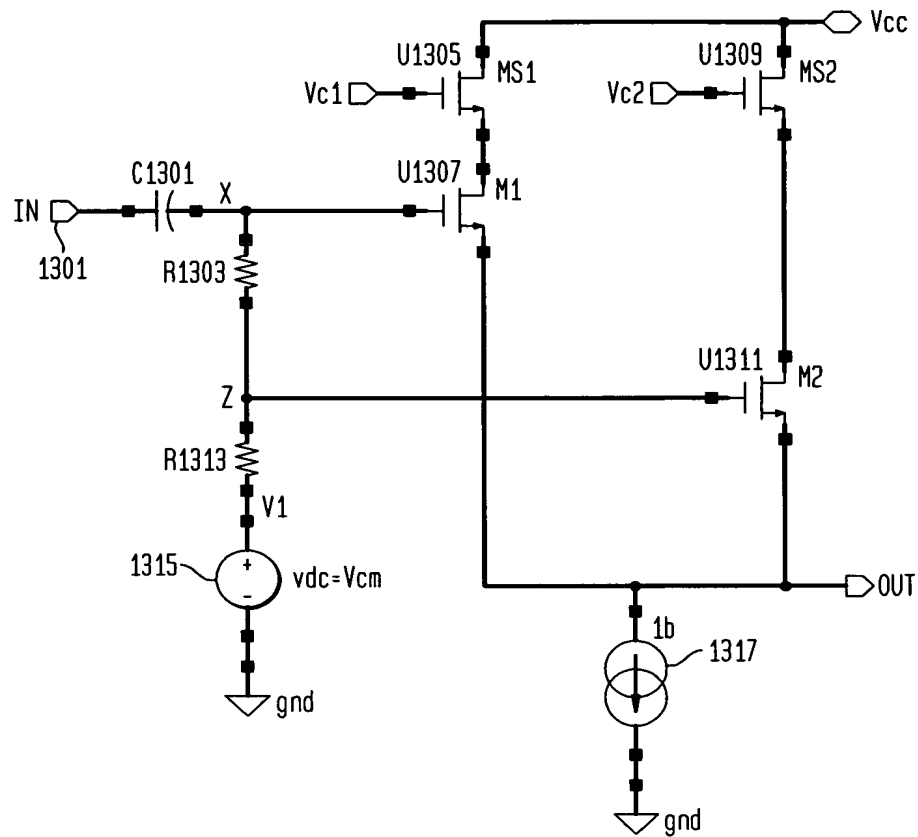


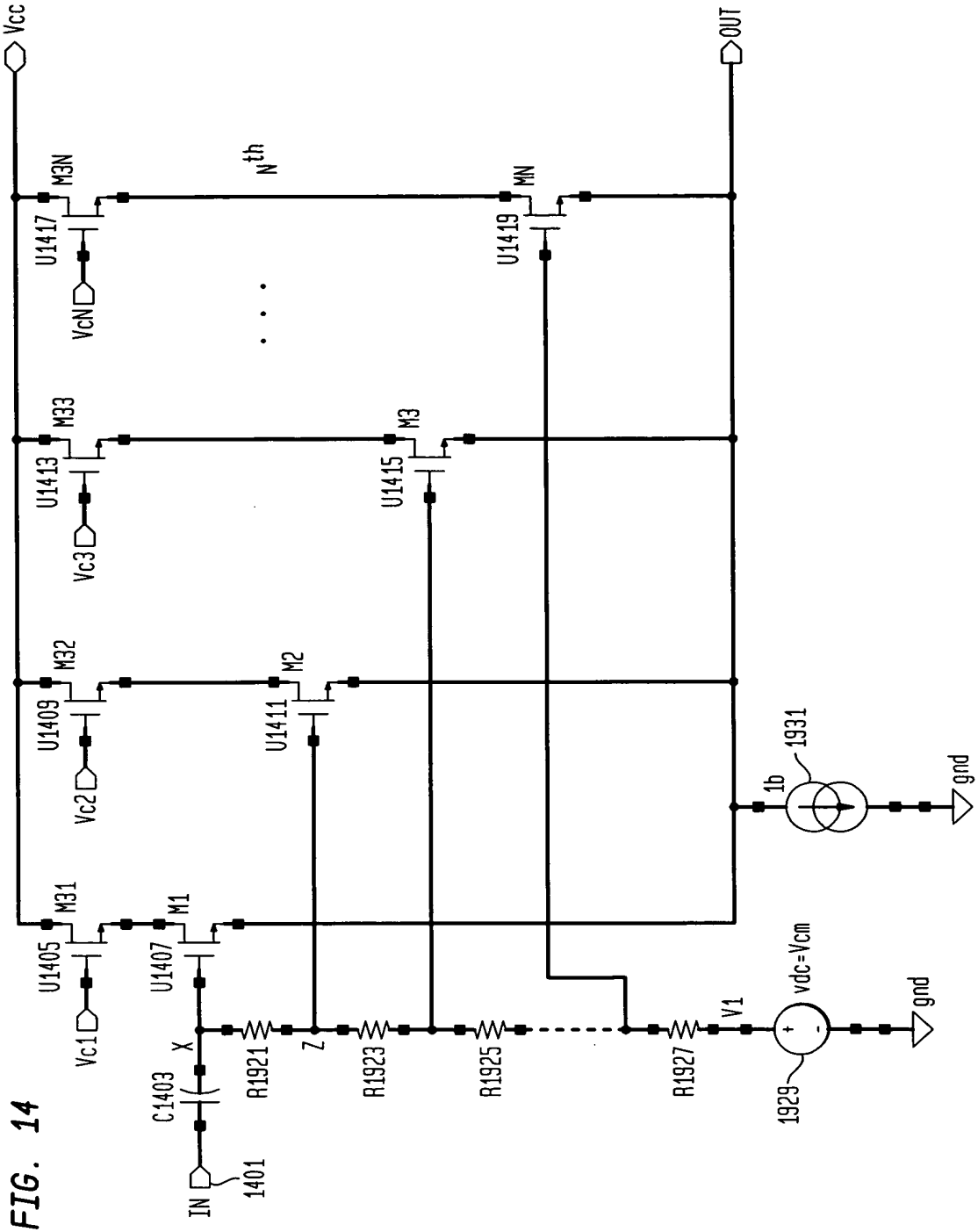
**FIG. 10**  
 (PRIOR ART)

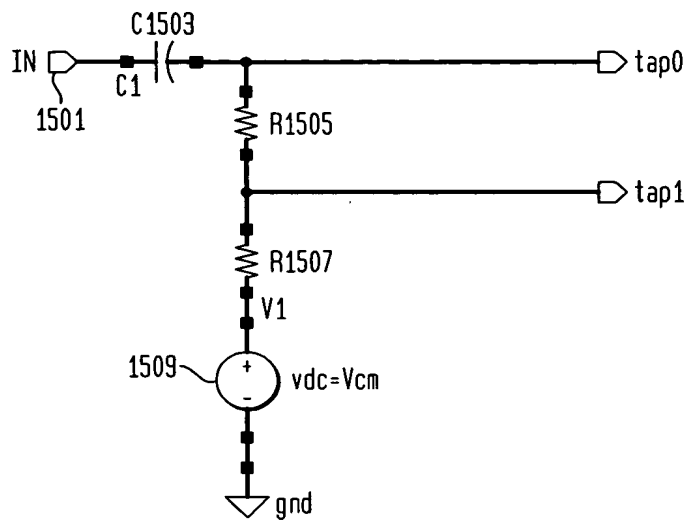
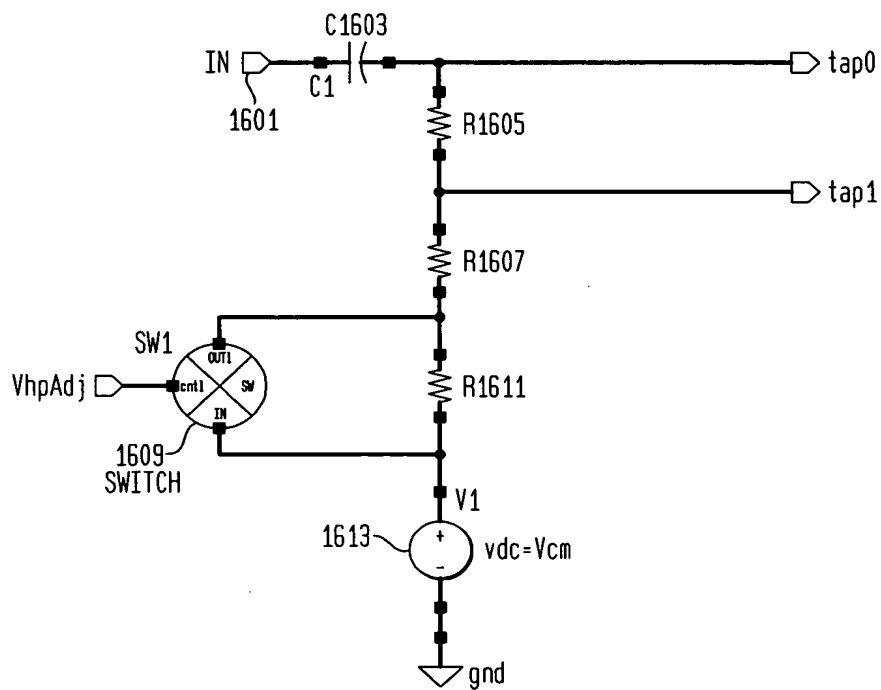


**FIG. 11****FIG. 12**



**FIG. 13**



**FIG. 15****FIG. 16**

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 Title: Adjustable Bandwidth High Pass Filter for Large Input  
 Signal, Low Supply Voltage Applications

FIG. 17

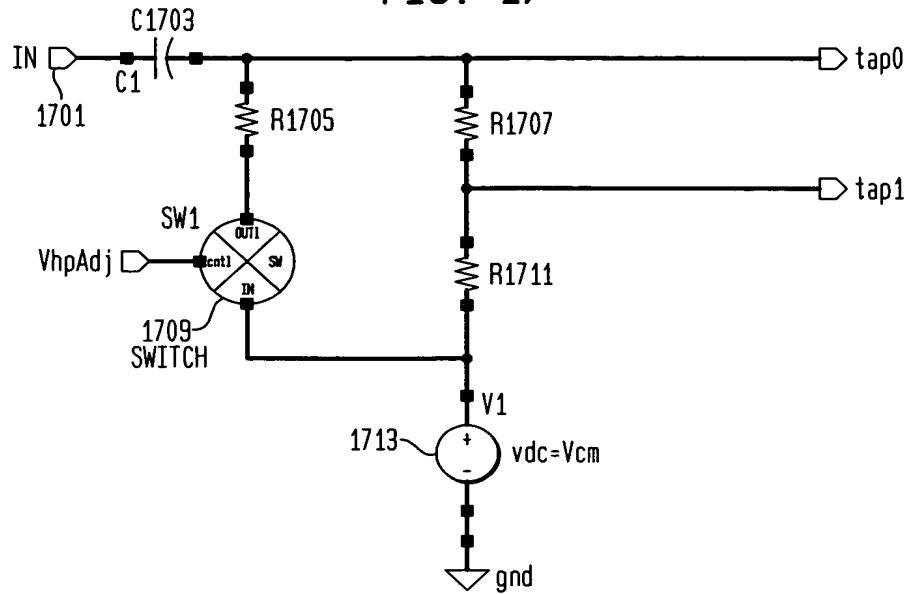


FIG. 18

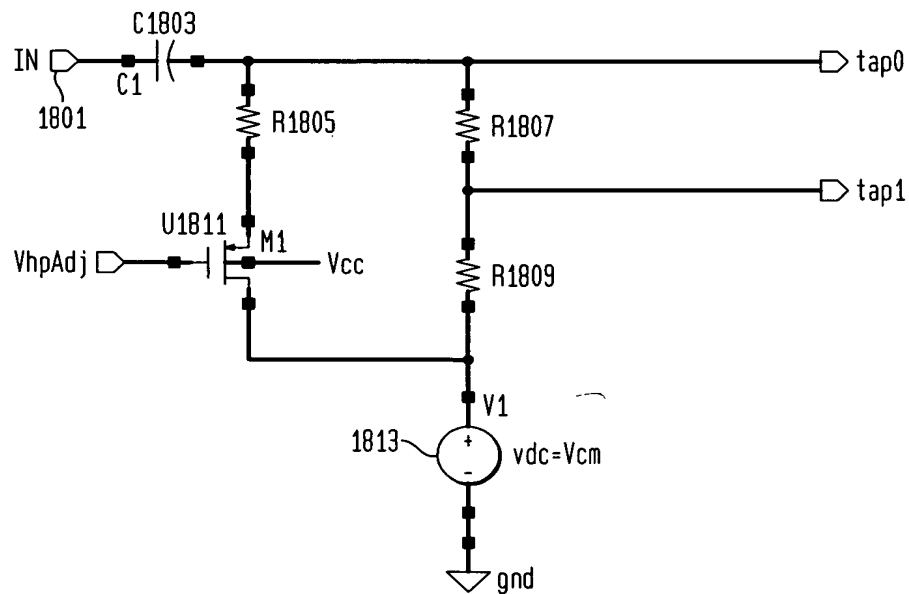
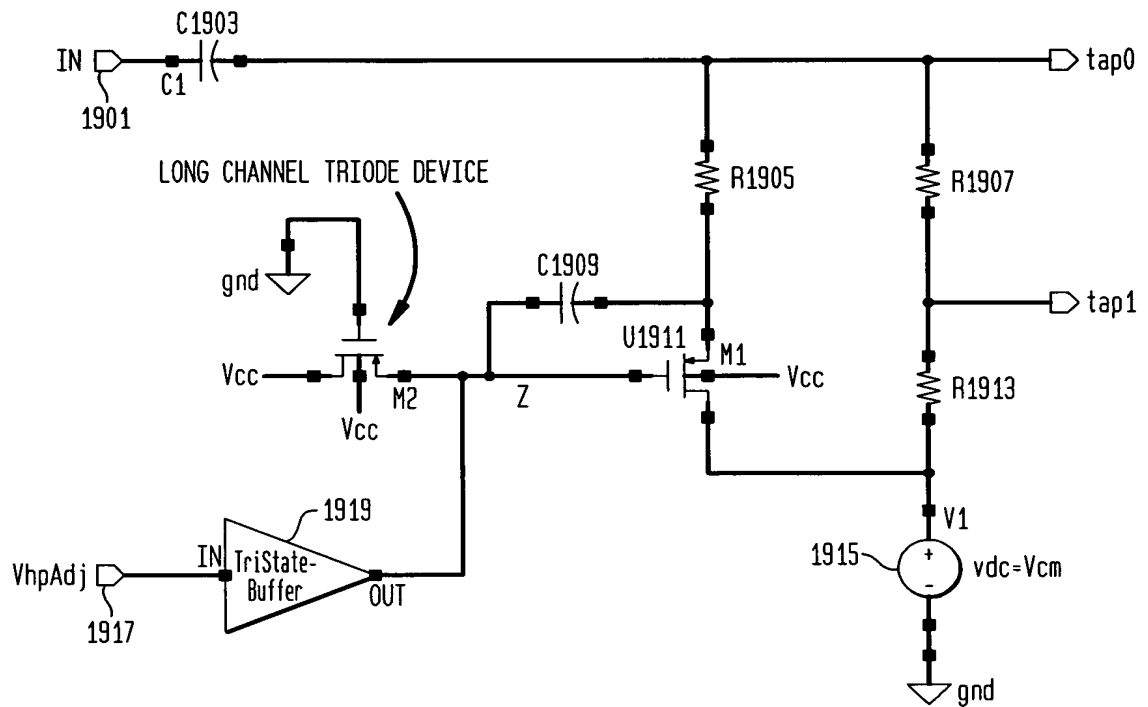


FIG. 19





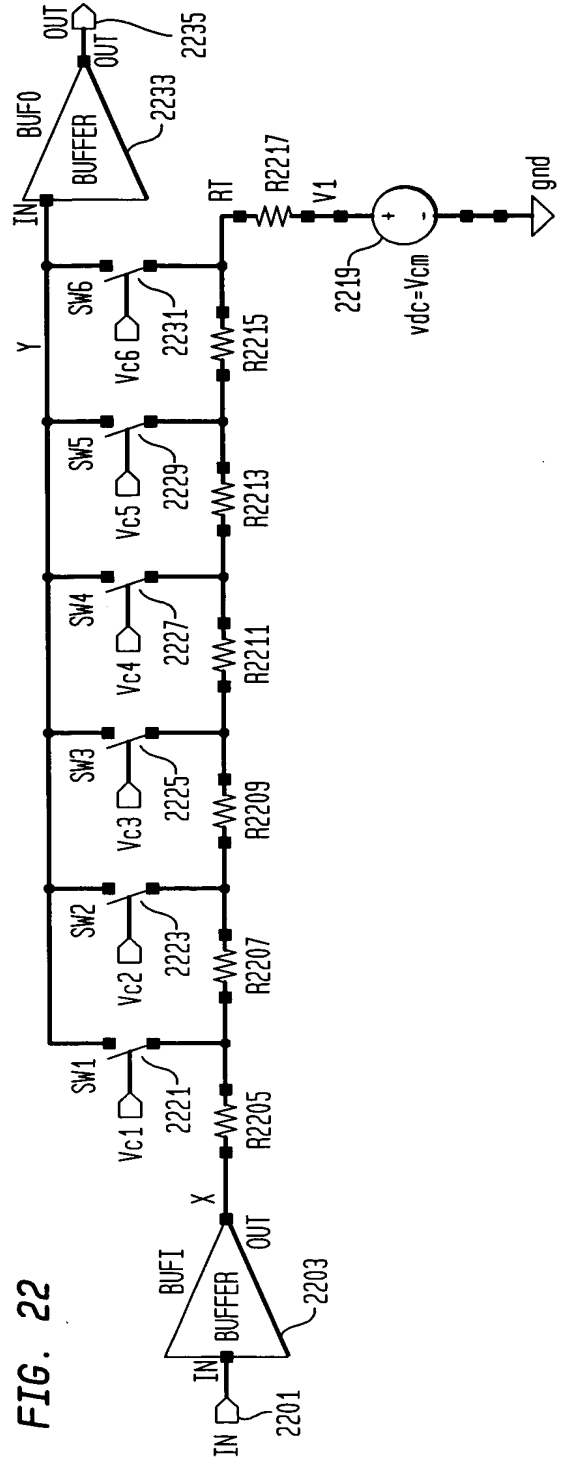
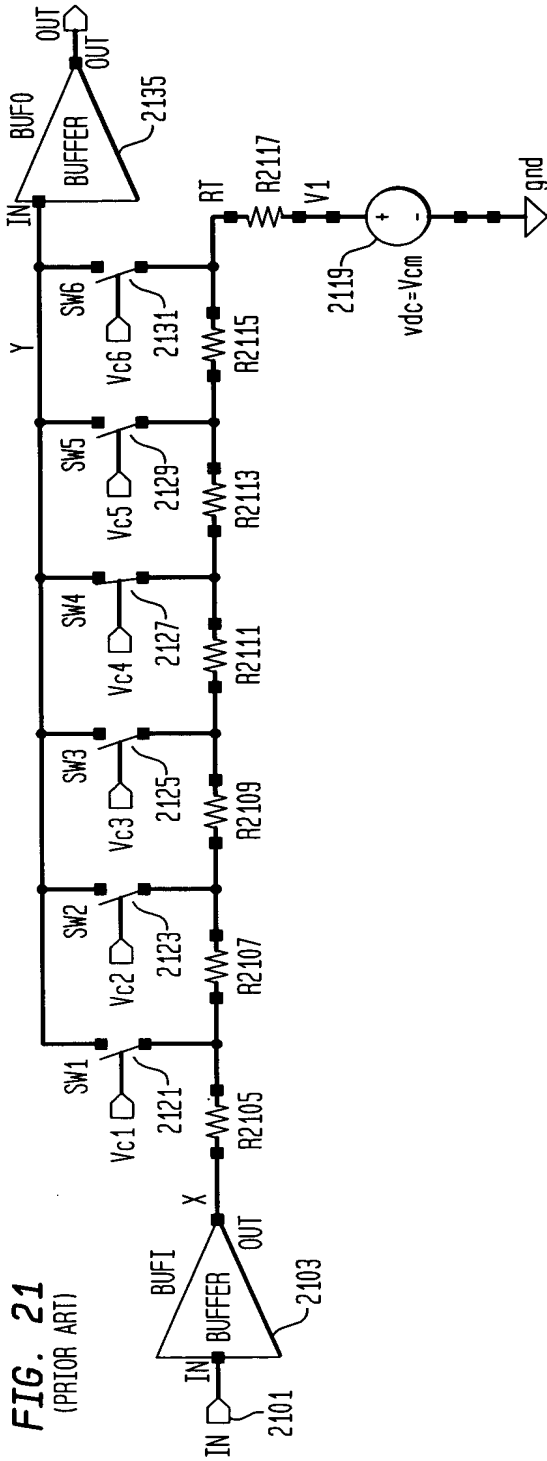
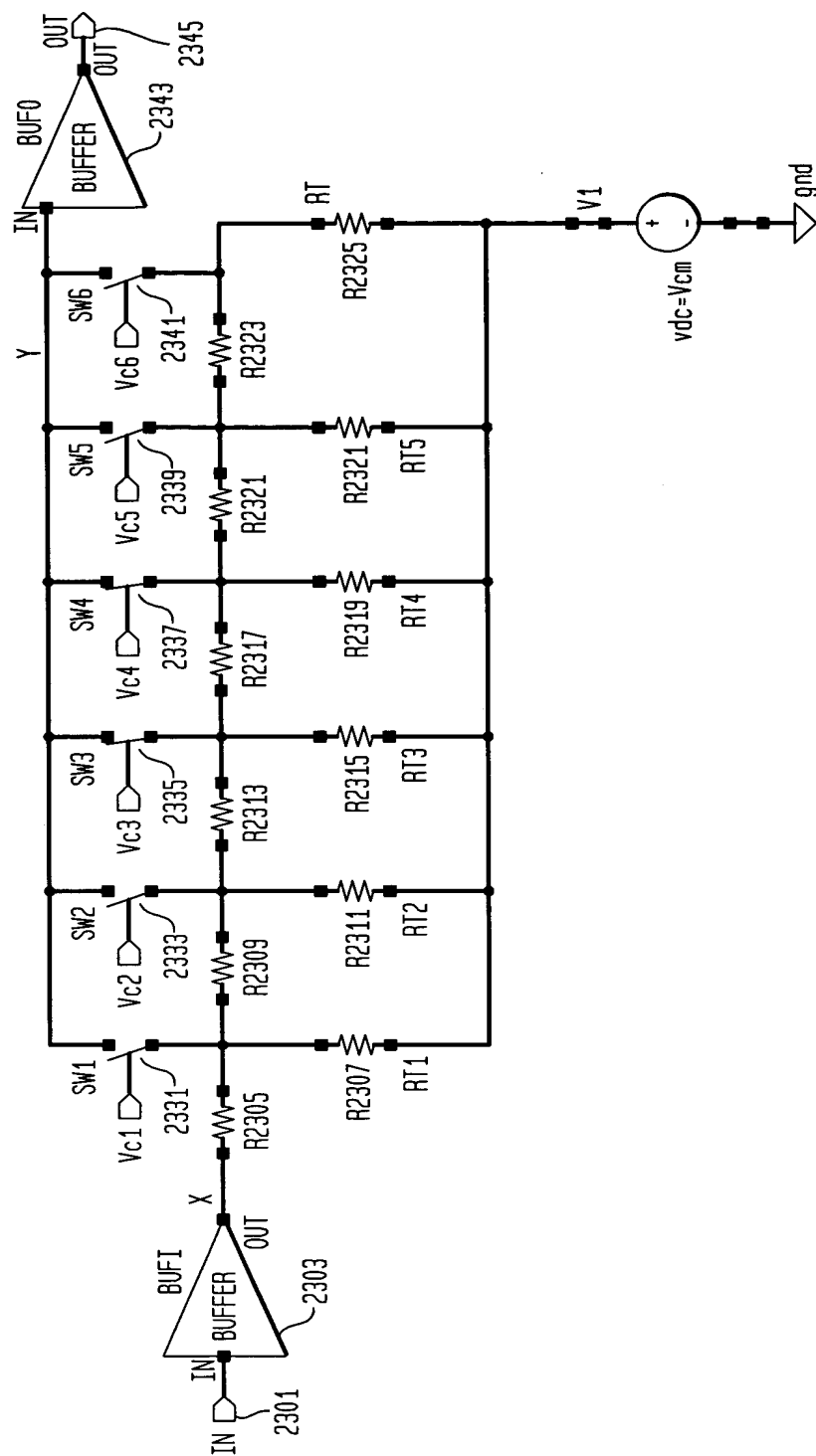


FIG. 23





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FIG. 24

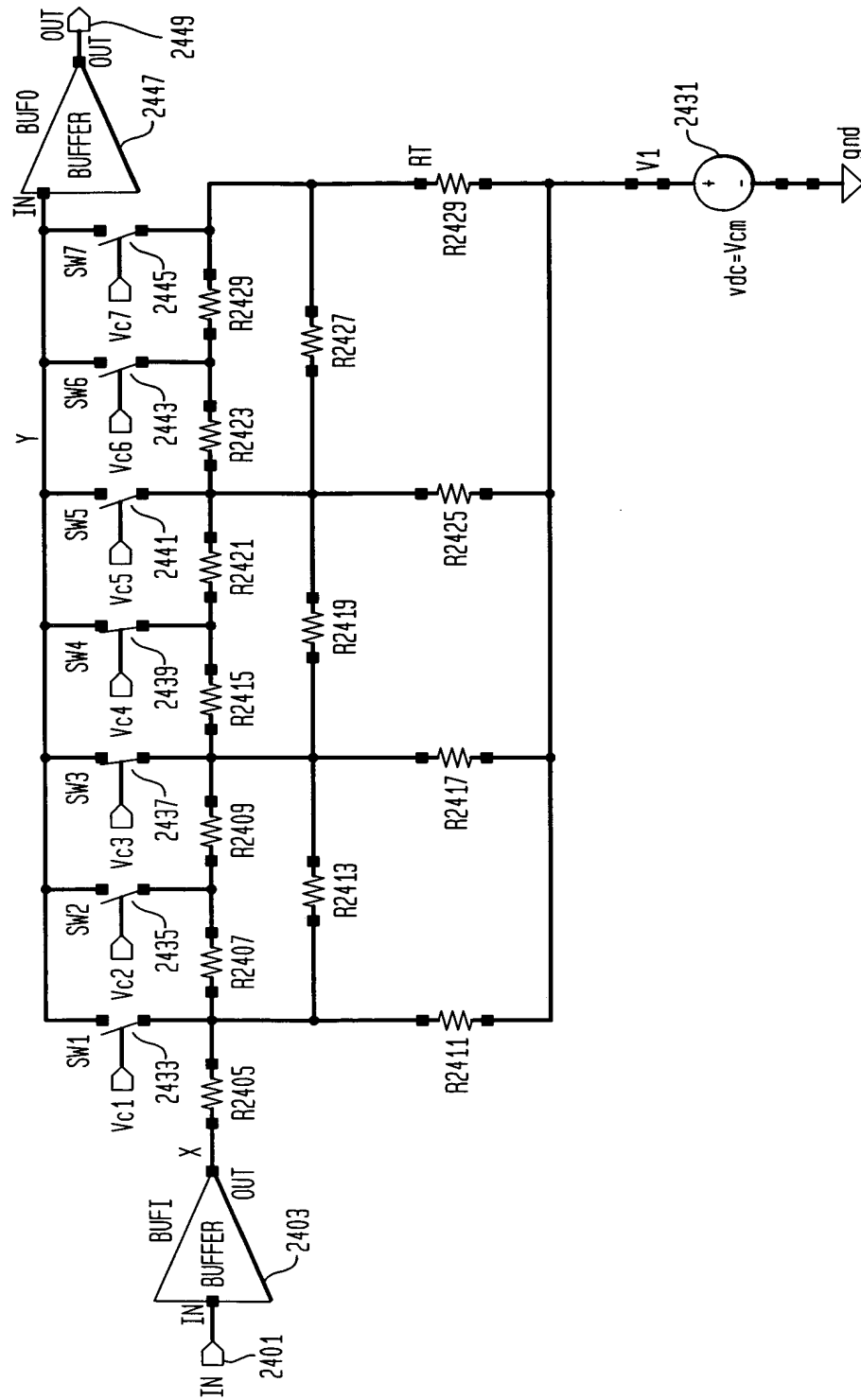


FIG. 25

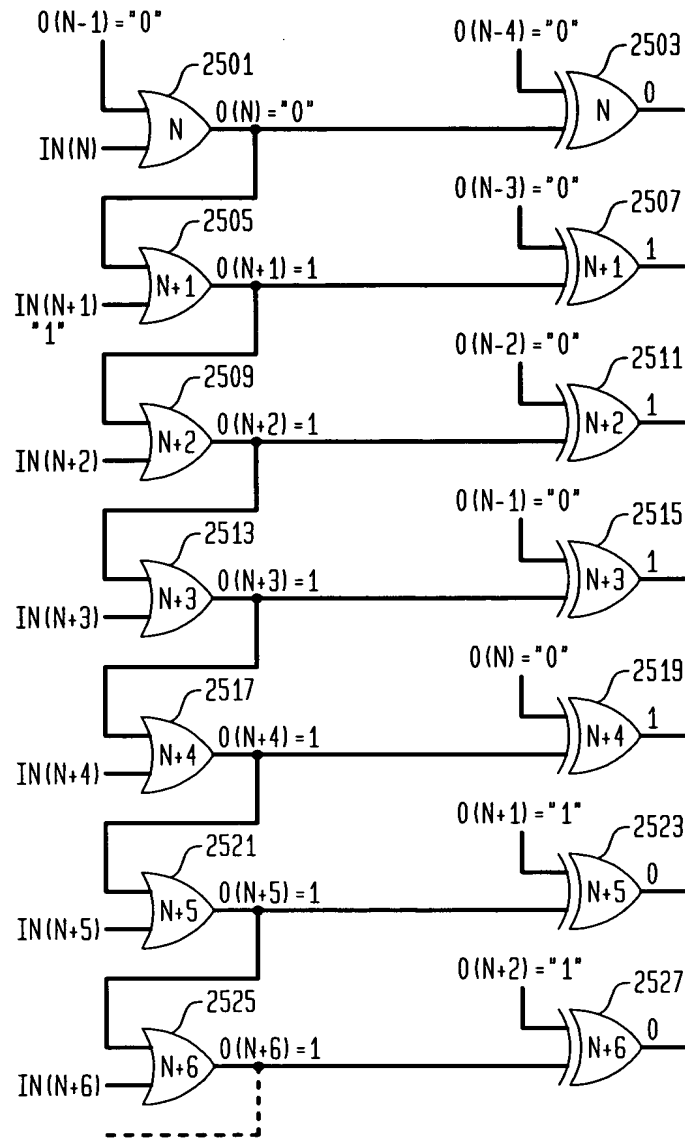
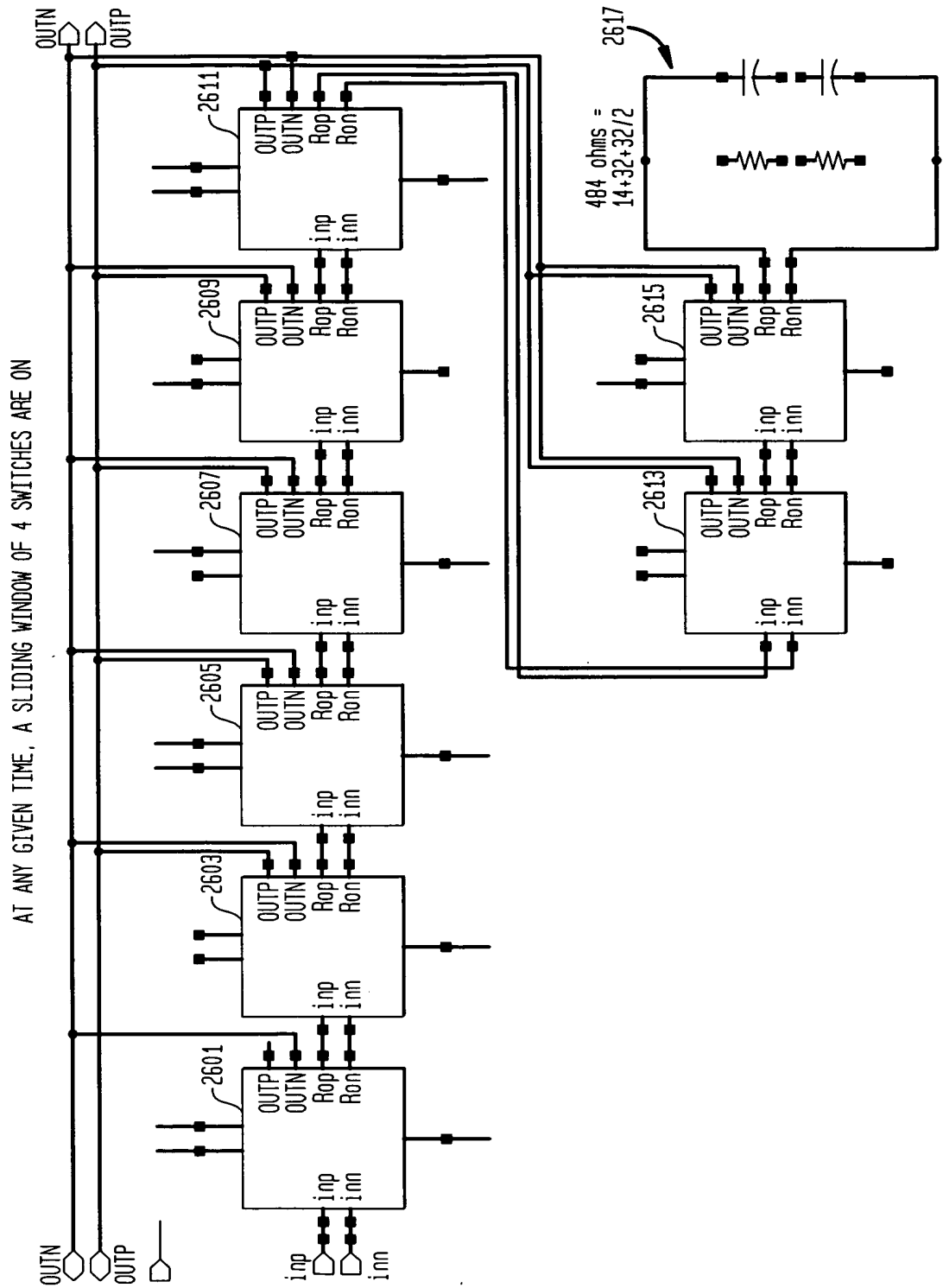
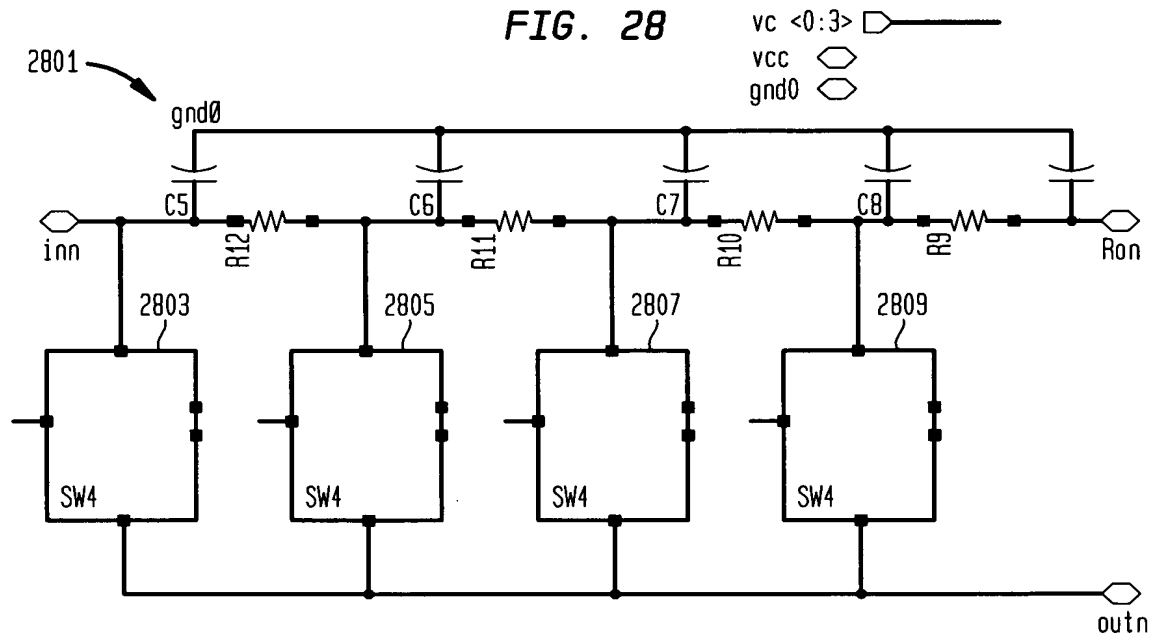
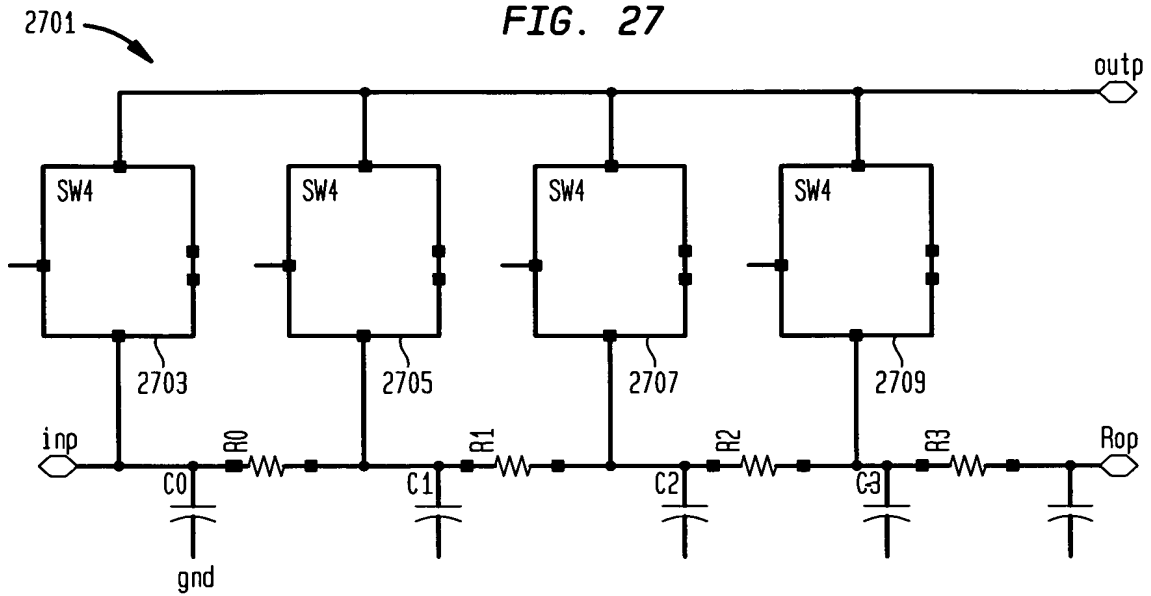


FIG. 26

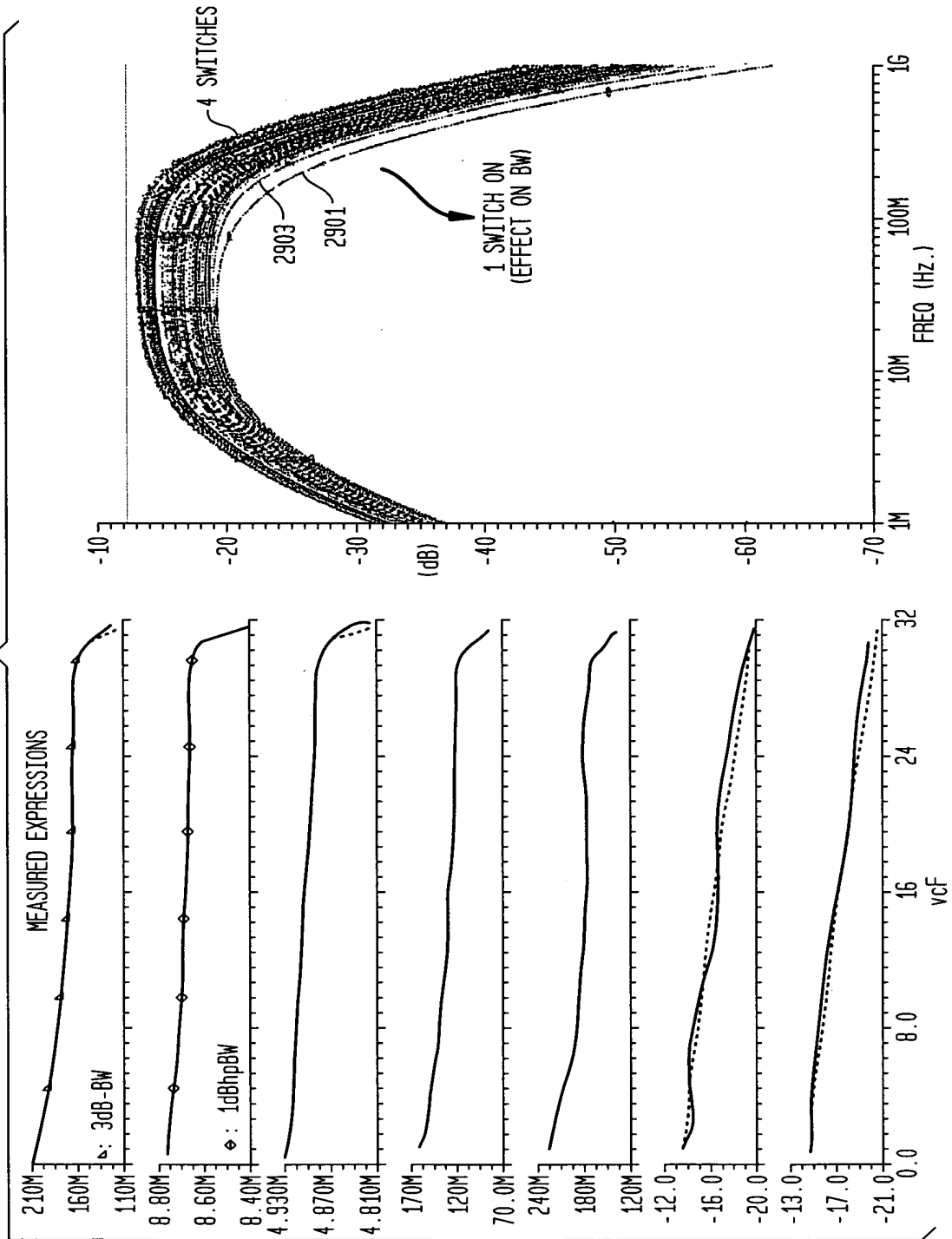


SWITCH SIZING:  
 N:  $w=1.8\mu$ ,  $L=0.25\mu$ ,  $m=2$   
 P:  $w=2\mu$ ,  $L=0.25\mu$ ,  $m=8$

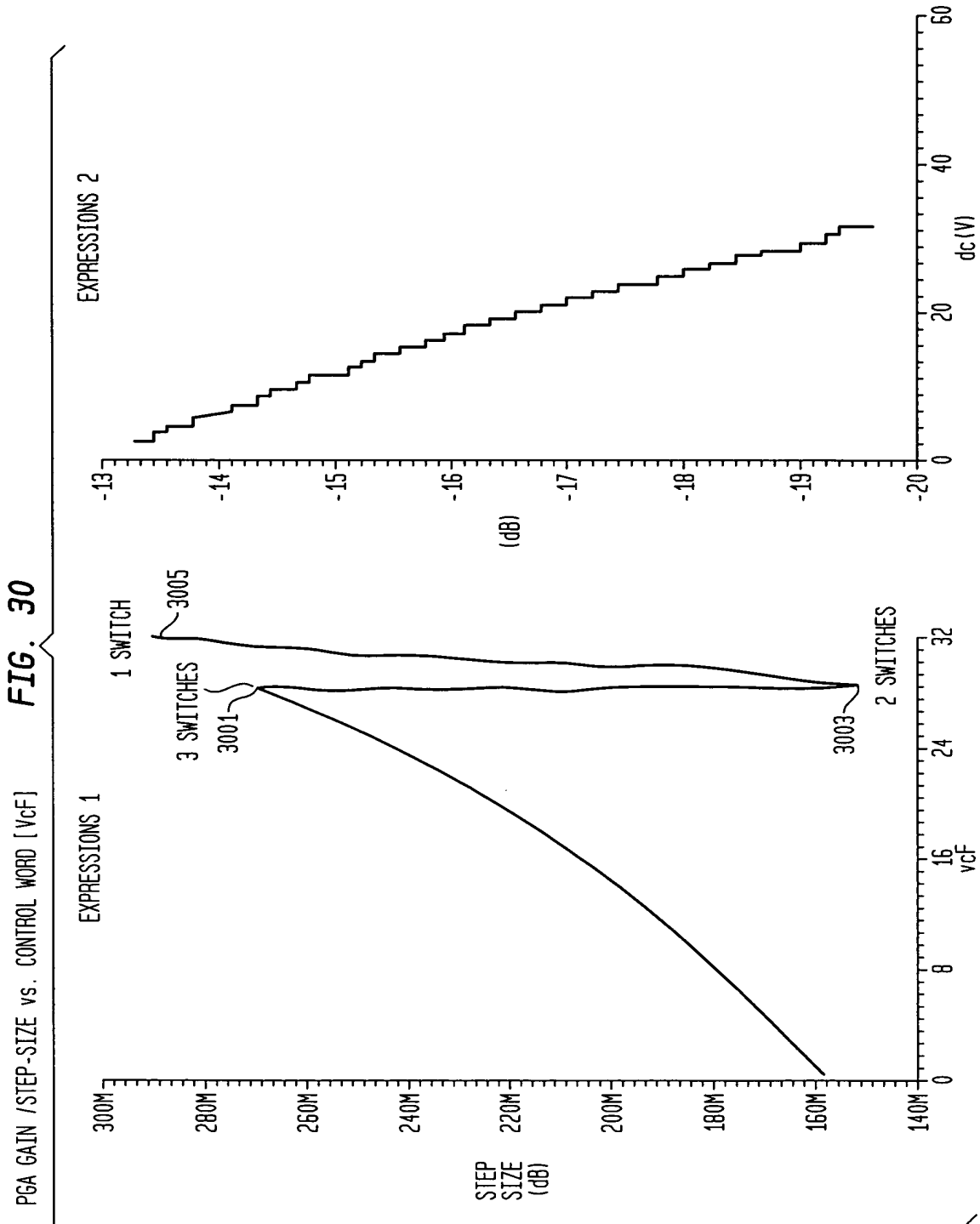


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FIG. 29

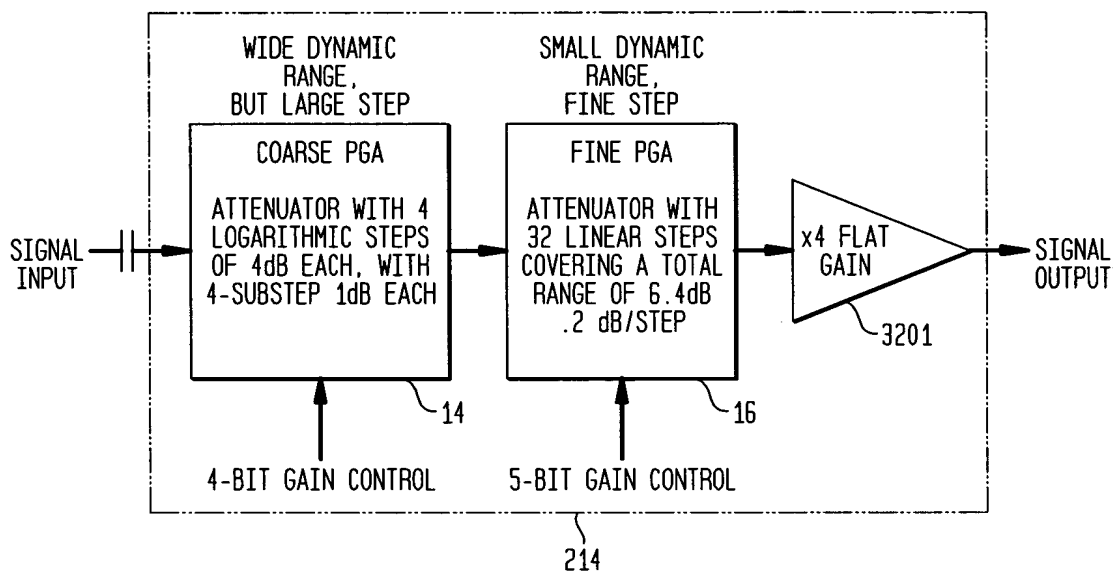


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**FIG. 31**

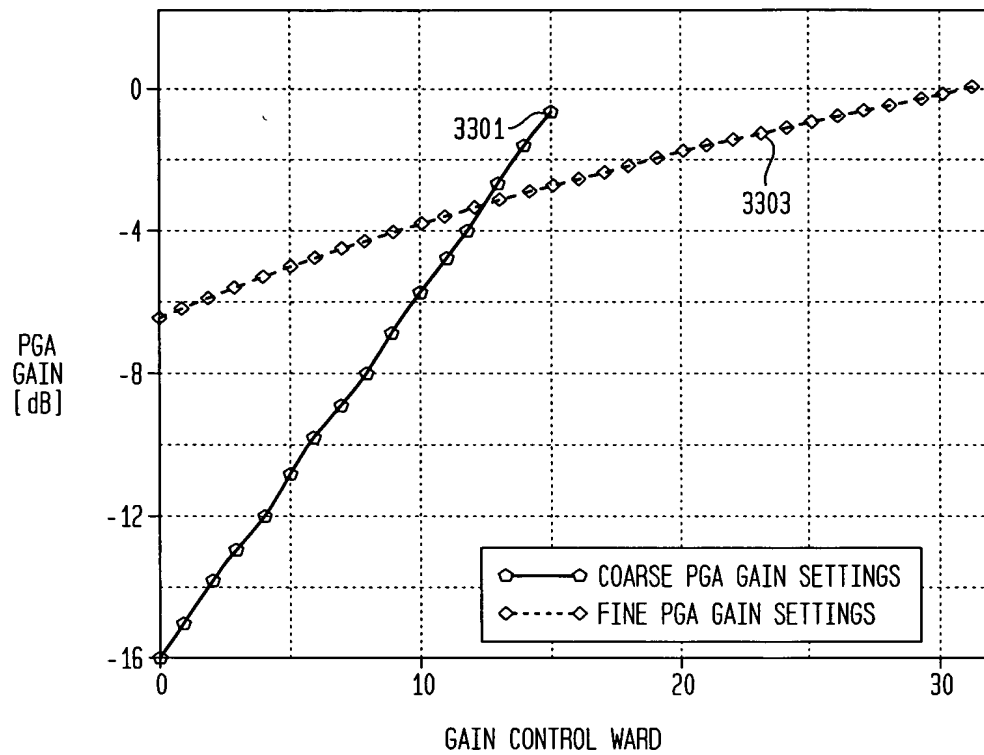
PROGRAMMABLE GAIN AMPLIFIER (PGA)



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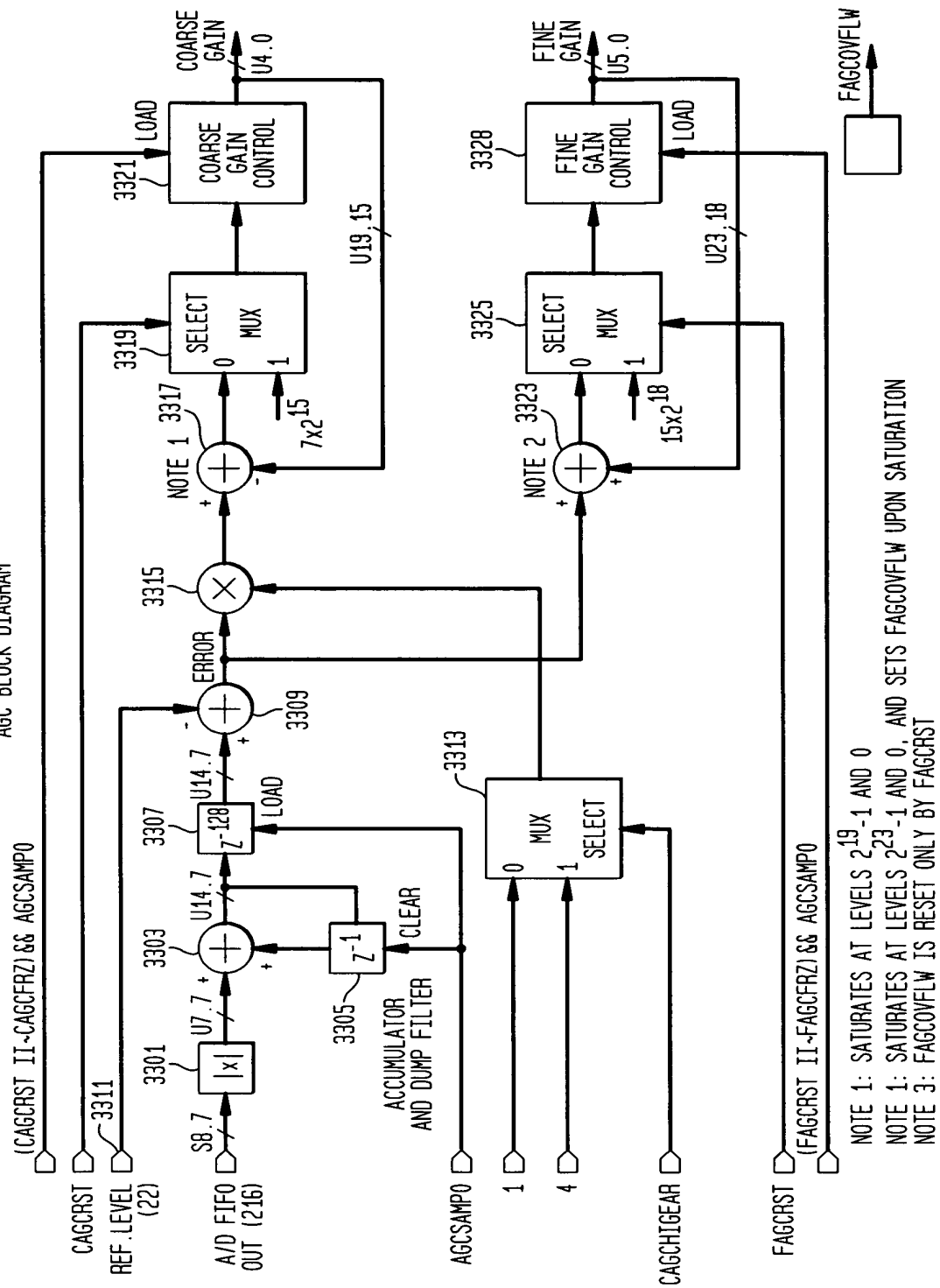
**FIG. 32**

COARSE AND FINE PGA GAIN SETTINGS





### AGC BLOCK DIAGRAM



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### FIG. 34

PEAK TO RMS RATIOS FOR 100Base-TX AND GIGABIT

CABLE LENGTH [m]	100Base TX	GIGABIT, 100 OHM	GIGABIT, 85 OHM	GIGABIT, 115 OHM
0	3.691281	4.193192	4.193192	4.193192
20	3.806628	4.501316	4.362110	4.291369
40	3.877284	4.528136	4.457336	4.429949
60	3.894216	4.733644	4.695307	4.646305
80	4.055372	4.878569	4.847844	4.810019
100	4.225522	4.983545	4.991296	4.968900
120	4.357733	5.134131	5.194401	5.154263
140	4.556012	5.266919	5.380943	5.366309
160	4.764462	-	-	-

$$\begin{aligned} \text{TARGET } E\{|x|\} &= \text{A/D CLIPPING LEVEL} \times (E\{|x|\}/\text{RMS}) / (\text{PEAK}/\text{RMS}) \\ &= 127 \times 0.7979/5.2 = 20 \end{aligned}$$